gelato ICE

Itanium® Conference & Expo | 2007

Spotlighting Linux® on Itanium®-based Platforms

April 15–18 | San Jose, California | USA

Welcome!

Brought to you by:

gelato.org

Thank you !

- The Gelato Central Operations Staff
- The Program Committee
- Our Speakers who are volunteering their time
- Our Attendees
- Conference Sponsors (HP, Intel, and the Itanium Solutions Alliance)
- Media Sponsors (HPC Wire, GRIDToday)
- University of Illinois (where the Gelato Central Operations team is hosted)

The IT World is Changing

- The multi-core transition
- What happened to the end of Moore's Law?

  Hafnium/metal gate based process → 45nm (2008), 32nm (2010) and beyond?

Good News for Itanium

- Full alignment on design tools and process for the Tukwila release (per Gelsinger's March interview)
- Montecito is currently at 90nm and Itanium has great potential for increased silicon density for more cores, more cache, and frequency scaling headroom
- Gains in performance per watt and reduced cooling costs

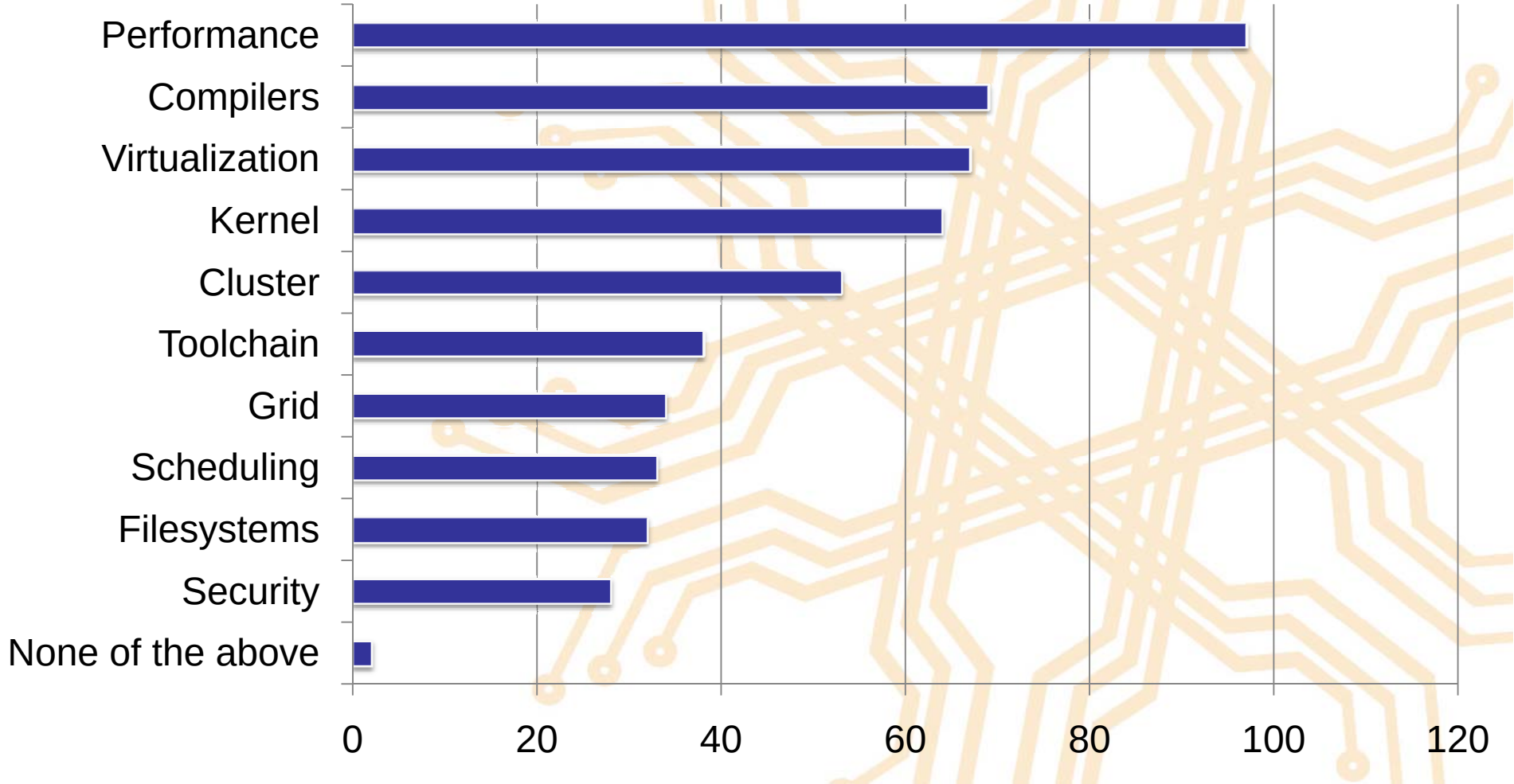
Why Gelato ICE?
Advancing Linux on the Itanium Platform

Collaboration

Education & Support

Community

ICE San Jose 2007
Attendee Interest Areas
(multiple responses per attendee)



Gelato ICE Highlights

- Itanium
  - **Keynote:** Enterprise Workloads on Itanium-based Servers (Bozman, IDC) – Mon. AM
  - Itanium Processor Vision and Roadmap (Fister, Intel) – Tues. AM
  - **Keynote:** Itanium, A Popular Platform for Large Systems (Coekaerts, Oracle) – Wed. AM
  - Setting up a Quiet Itanium-Based Home Office for Fun and Profit (Mosberger) – Wed. PM

Highlights (cont)

- Linux
  - GCC Track – Mon. & Tues.
  - **Keynote:** Linux Kernel Development for the Itanium Architecture (Morton) – Tues. PM
  - IA-64 Linux Kernel Track – Tues. PM & Wed.
  - Distribution Panel – Wed. PM

Highlights (cont)

- Multi-core
  - The Significance of Multi-core: The Intel Perspective (Tian, Intel) – Mon. PM
  - Multi-core Programming & Research, The Future of Itanium (Hwu, UIUC) – Mon. PM
  - Multi-core Programming Workshop and Lab – Tues. PM & Wed.

Highlights (cont)

- Other
  - ISA Developer Days Track – Mon.
  - General Interest – Mon. AM & Tues. AM
  - Virtualization Track – Mon. & Tues. AM
  - Tools and Tuning Track – Tues. & Wed. PM
  - Topics for Enterprise – Wed.
  - Research / Advanced Topics – Mon. PM, Tues. PM, & Wed.
- Social: Luau and Hawaiian shirt contest – Tues. Evening

(IP)2 Award Winner

Title: Hardware Profile-Guided Automatic Page Placement for ccNUMA Systems

- *Gelato Member:* North Carolina State University
- *Researchers:* Jaydeep Marathe and Frank Mueller
- *Presentation Time:* Wed., April 18, 12:00-12:45, IA-64 Kernel Track
- Selected by the Gelato ICE Program Committee as project that will have a potentially great impact on the Itanium platform.

Overview: Intelligent page-placement policy that allocates pages closer to the requesting processor to improve wall-clock execution time (up to 20% on tested benchmarks)

The Community behind Gelato ICE, The Gelato Federation

Gelato is the global technical community dedicated to advancing Linux® on the Intel® Itanium® platform through collaboration, education, and leadership.

Founded January 2002

The Gelato Federation

Membership:

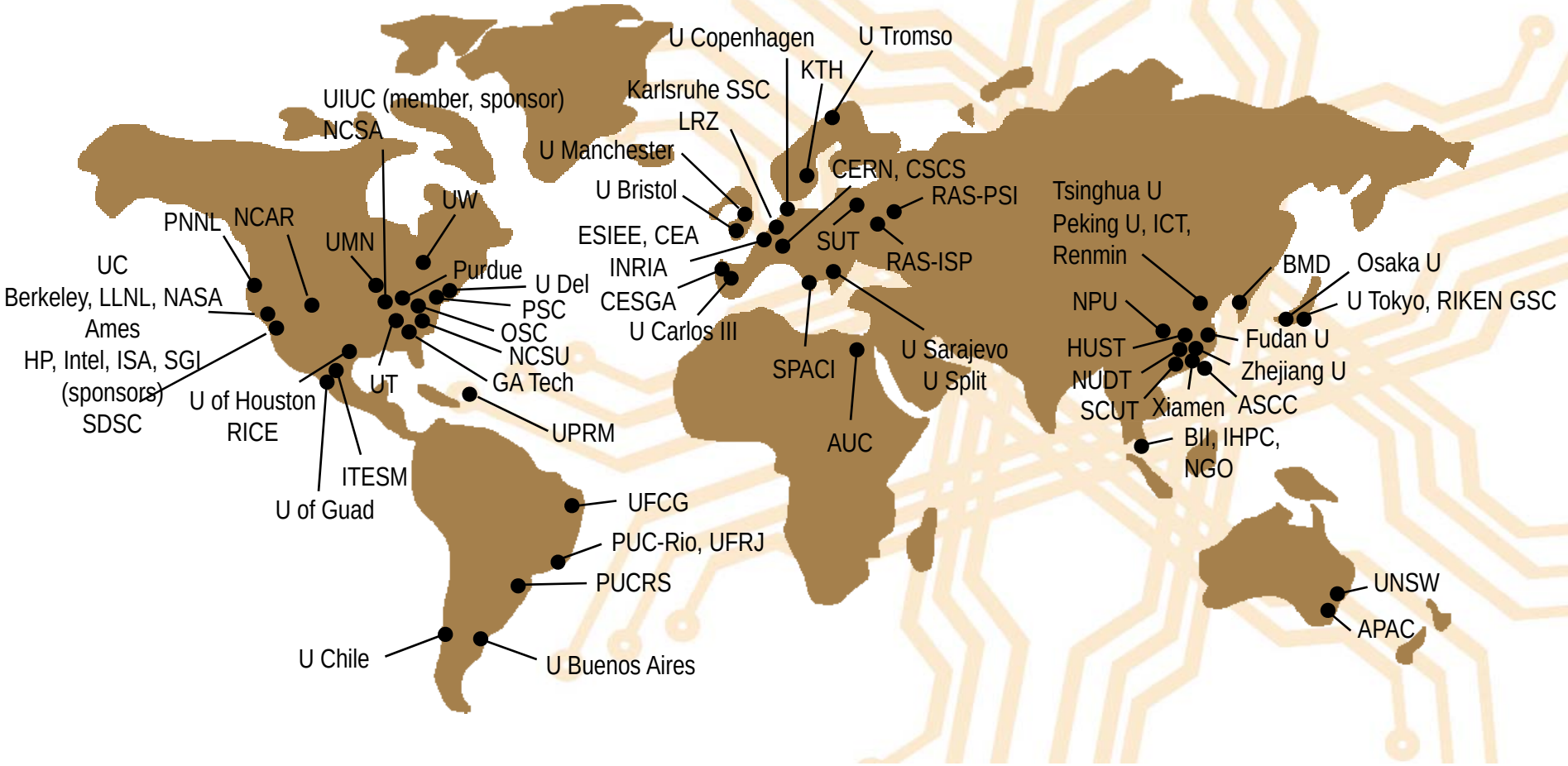
- Seventy members as of today
- The Gelato Federation is a very diverse group - suppliers and users of Itanium Linux technology and solutions

Sponsors:

- HP (founding sponsor)
- Itanium Solutions Alliance
- U of Illinois (host sponsor)
- Intel
- SGI

Gelato Membership April, 2007

70 Members, 5 Sponsors



What is Gelato Role?

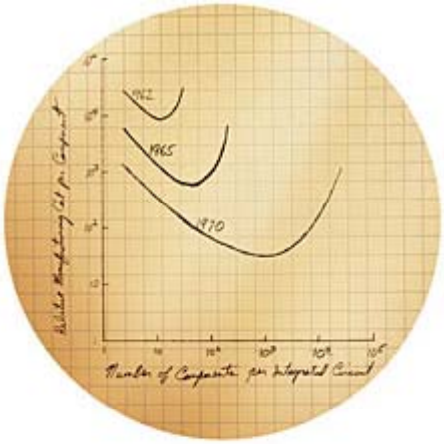
- Provide expertise to help address Linux-Itanium-related programming and research challenges
- Engage relevant technical communities and provide technical leadership in those communities

Itanium's Future:

Scalability for the Long-term in a Multi-core World

40 Years of Moore's Law

(transistor density doubles every 18 to 24 months)



- Processor performance gains have been tied to increasing transistors densities and corresponding increases in clock frequency
- Power consumption and heat dissipation are now limiting factors in processor designs
- Increasing clock frequencies is no longer viable as the primary means for boosting processor performance

Ways to use transistor density to boost performance

- Larger Data Formats
- Instruction Level Parallelism (ILP)
- Hyper-Threading
- Larger Cache

These strategies **will not** deliver the kinds of performance gains that have been delivered in the past by frequency ramping.

Ways to use transistor density to boost performance: Moving to multi-core

- Integrate more execution cores into each processor
- Turn down clock frequencies to contain power consumption and heat generation

Multi-core advantages

- Faster core-to-core communications
- Dramatic throughput increase for multi-threaded software

* Additional cores in a multi-core processor deliver **little or no benefit for a single-threaded application running on a dedicated server**

What about Itanium?

- Designed to deliver new levels of parallelism
- Enable sustainable performance ramping without relying on ever-higher clock frequencies --- "*doing more per clock cycle*"

EPIC relies on the compiler to ...

- Find and explicitly identify independent instructions
- Look thousands of instructions ahead to find additional opportunities for parallelism

The compiler is not limited by the time and resource constraints of dynamic, hardware-based ILP optimization.

Itanium Advantage – Per core performance

- ILP not performed in hardware - ability to support increasing ILP through compiler optimization
- Reduces the need for long instruction pipelines and a lot of complex, energy-consuming logic circuits
- Itanium has a relatively small, high-performing and very power-efficient core

Itanium Advantage – more cores possible

- It is easier to integrate more cores per processor in the future, while leaving plenty of space and power for large cache configurations.
- Increasing ILP through compiler optimization combined with its advantages for multi-core implementations, this provides **strong potential for performance scaling**.

Itanium's Future: Scalability for the Long-term in a Multi-core World

- more parallelism per processor (EPIC)
- increasing ILP through future compiler improvements
- more cores per die possible lowering power consumption and providing ample space for large, on-die cache
- more frequency scaling performance possible (90nm → 65nm → 45nn → 32nm)

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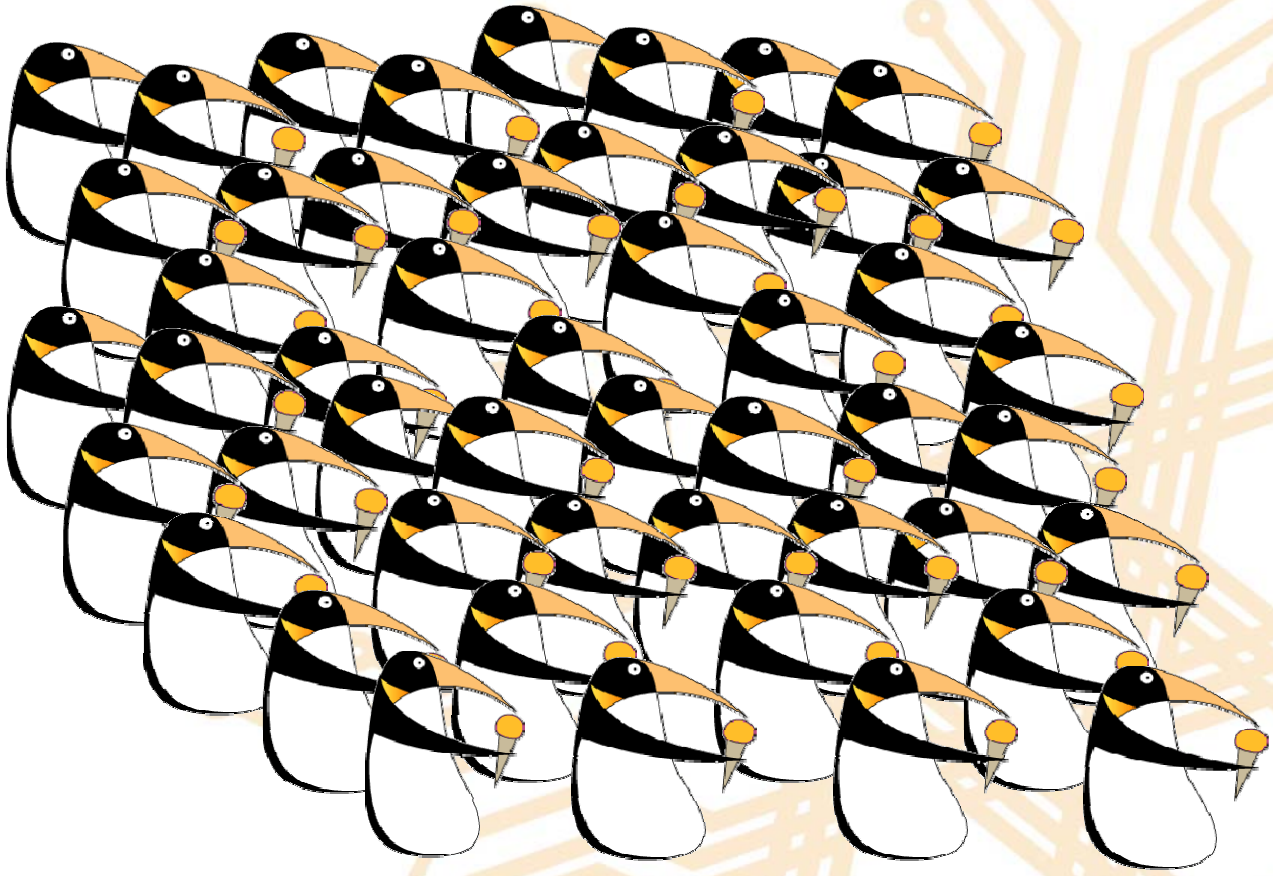

Let’s have a great meeting!